Technical Data

WATKINS-JOHNSON

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Digital Demodulator WJ-9482-1

(International Version)

Description

The WJ-9482-1 Digital Demodulator uses advanced digital signal processing (DSP) and surface mount technology to achieve high-performance precision demodulation of received signals in a compact, low-cost package. The unit accepts a 140-MHz IF input (160-MHz optional), performs demodulation of low- to high-rate PCM signals, and provides a decoded-symbol data output in a word parallel format. An input automatic gain control (AGC) circuit allows operation of the demodulator with an analog input level ranging from -30 to -10 dBm.

The WJ-9482-1's flexible DSP-based architecture allows the implementation of any IF bandwidth between 1 and 56 MHz. WJ's standard set of filters provides 96 bandwidths from 1 to 56 MHz.

The WJ-9482-1 supports BPSK, QPSK, SQPSK, 8 PSK, and 16 QAM demodulation modes. It also supports symbol rates up to 40 Mbaud, as well as a selection of absolute or differential encoding, and symbol-bit mapping. Sophisticated DSP-based adaptive algorithms provide acquisition and tracking of the symbol timing error, residual carrier offset, and equalizer tap updates. The WJ-9482-1 supports a 32-tap fractionally spaced T/2

Features

- ❏ *Low-cost precision demodulator*
- ❏ *BPSK, QPSK, SQPSK, 8 PSK, 16 QAM, demodulation modes*
- ❏ *140-MHz IF input (160-MHz optional)*
- ❏ *Input signal rates from 1 to 40 Mbaud*
- ❏ *Selectable absolute or differential encoding*
- ❏ *Self-training 32-Tap T/2-spaced adaptive equalizer (16-Tap for SQPSK)*
- ❏ *Flexible symbol-bit mapping*
- ❏ *Ethernet remote control*
- ❏ *Built-in test capability to detect faults to circuit card level*
- ❏ *1.75 in (3.86 cm) high full-rack package*

HEIGHT	1.75 in (4.44 cm)	**DEPTH***	20 in (50.26 cm)
WIDTH	19 in (48.26 cm	**WEIGHT**	20 lbs, max (9.05 kg

*** Excluding connectors & handles**

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equalizer for all demodulation modes, except SQPSK. For SQPSK, the unit supports a 16-tap T/2-spaced equalizer.

The WJ-9482-1's 32-bit microprocessor circuitry permits powerful local or remote control. An operator can transfer all control and status information through a TCP/IP-compliant ethernet interface. The unit's built-in test software allows location of faults to the circuit card level.

For all of its capability, the WJ-9482-1 is extremely compact and is contained in a single 1.75 by 19 by 20 inch (4.44 by 48.26 by 50.80 cm) rack-mount enclosure. The unit weighs approximately 20 pounds.

Functional Description

The functional block diagram in Figure 1 shows the standard and optional modules that make up the WJ-9482-1 Digital Demodulator. The unit accepts a 140-MHz IF input (160-MHz optional). A 56-MHz SAW filter band limits the input prior to conversion to baseband and digitization. An AGC circuit maintains an acceptable signal level into the analog-to-digital (A/D) converter that digitizes the analog input signal at a 162-MSPS rate with 8 bits of precision. The resulting digital baseband is then available for subsequent processing.

The digital demodulator subsystem incorporates three advanced very large-scale integration (VLSI) application-specific integrated circuits (ASIC), which are designed and optimized for wideband pulse code modulation (PCM) demodulation. These ASICs include:

- Digital filter chip for input filtering and adaptive equalization
- Digital resampler to digitally resample the input data at a rate synchronous with the baud rate
- Digital mixer chip to remove carrier offsets

Incorporating these ASICs provides a significant size, cost, and complexity savings.

After digitization, the WJ-9482-1 digitally performs all the remaining processing functions. The demodulator filters and decimates the digital baseband commensurate with the desired baud rate. This extracts the desired signal, and eliminates out-of-band signals and excess noise. Applying additional AGC optimizes the inband signal power. The unit then synchronously resamples the predetected data stream at exactly twice the baud rate. A 32-tap T/2-spaced complex adaptive equalizer accepts the baud-synchronous data and generates the equalized symbol data at the baud rate. (NOTE: For the SQPSK demodulation mode, the equalizer is a 16-tap T/2-spaced complex adaptive equalizer that continues to output data at twice the baud rate.) Finally, a carrier-removal ASIC removes any residual carrier offset in the resultant symbol data and performs symbol alignment for SQPSK. The Output Formatter Module carries out the final symbol estimation, performs the appropriate symbol decoding, and outputs the demodulated symbols.

The WJ-9482-1 provides symbol-timing loop, carrier-recovery loop, and equalizer-tap update algorithms on three general-purpose DSP processors. This approach allows optimization of the algorithm implementations for specific modulation formats. It also allows significant flexibility in controlling loop dynamics during the acquisition and tracking phases. The processors provide analysis data including:

- Actual baud rate
- Actual residual carrier offset
- Signal quality estimate
- Snap-shot data representing the demodulated constellation

A 32-bit control processor provides overall control of the unit. In particular, the microprocessor carries out initialization, built-in test, and input/output of control and status through the ethernet interface.

System Applications & Options

Several WJ-9482-1 features facilitate the integration of the unit within a system. The modular construction allows easy maintenance with a minimum of down-time. A thorough built-in test capability permits the quick detection and isolation of hardware faults to the circuit card level. The basic WJ-9482-1 configuration accepts a 140-MHz IF input and provides decided-symbol data output. Options include a 160-MHz IF input capability (WJ-9482/160).

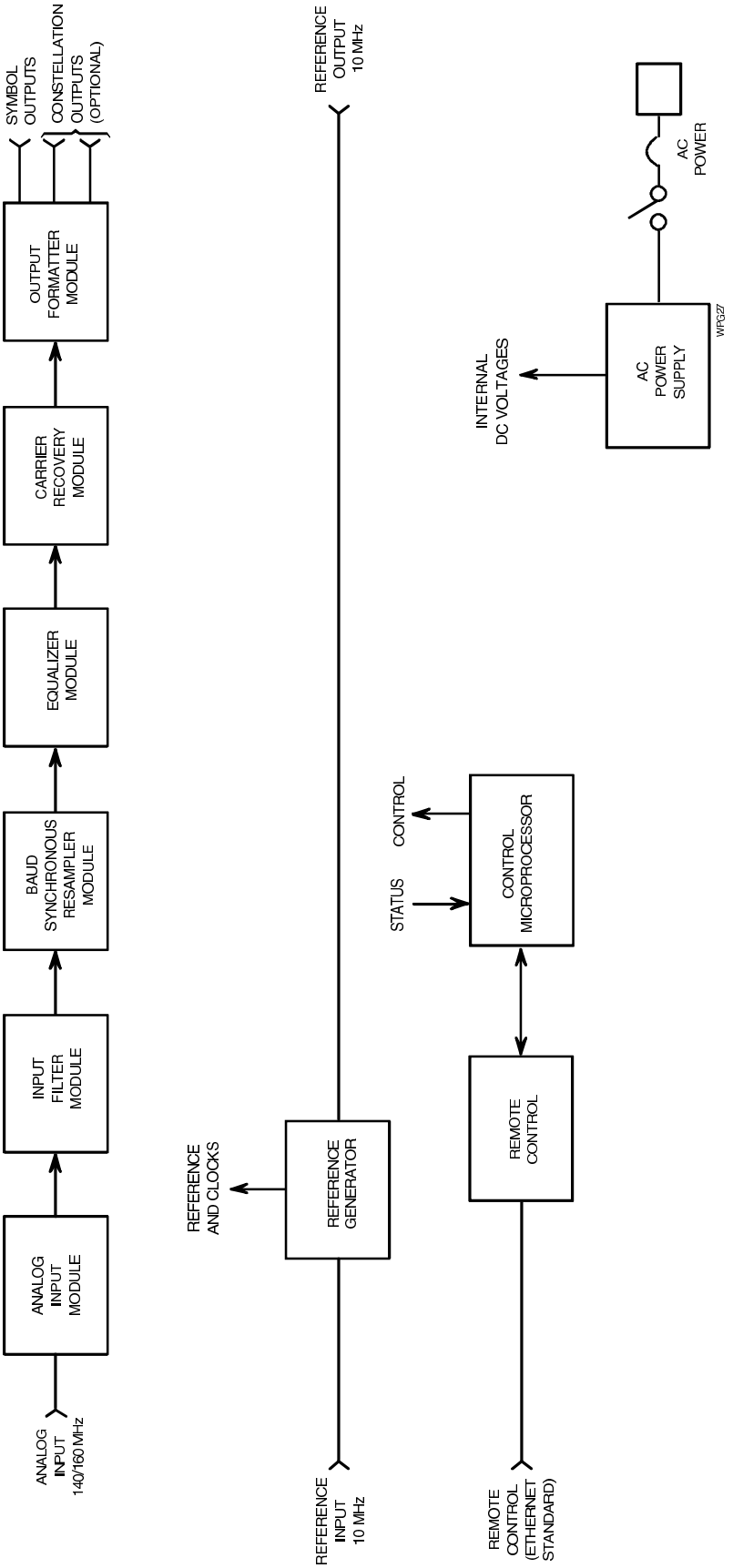

Figure 1. WJ-9482-1 Functional Block Diagram

Specifications

Analog Input Characteristics	
IF Input	140 MHz (160-MHz optional)
Bandwidth	56 MHz
Input Levels	-30 to -10 dBm
Noise Figure	22 dB, max
Input VSWR	2:1, max
Input Overload	+20 dBm, with no damage
Input Impedance	50 ohms
Image Rejection	60 dB
Gain Control	Manual or automatic
Manual Gain Control Range	30 dB
Demodulator Characteristics	
Detection Modes	BPSK, QPSK, SQPSK, 8 PSK, 16 QAM
Baud Rates	1 to 40 Mbaud
Equalization	CMA for acquisition, DD for tracking
Equalizer Taps	32 (16 for SQPSK)
Tap Spacing	1/2 symbol period
Digital Output Characteristics	
Symbol Format	N data bits with baud clock, where N = number of bits per symbol
Output Levels	Differential 10 k ECL
Output Clock	Data valid on falling edge (clock duty cycles = 50% $\pm$5%)
Output Connector	50-pin D
Control	
Remote	Ethernet AUI
Frequency Reference	
Internal Reference Stability	1 x 10^{-6}, max
Extrnal Reference Input	10 MHz, 200 mV into high impedance
Physical/Environmental	
Operating Temperature Range	0 to 50°C
Altitude	15,000 ft (4,572 meters) max
Power Requirement	85 to 264 Vac, 47 to 440 Hz
Power Consumption	115 W, max